A Distributed Parallel Embedded System for Autonomous Sonar Arrays

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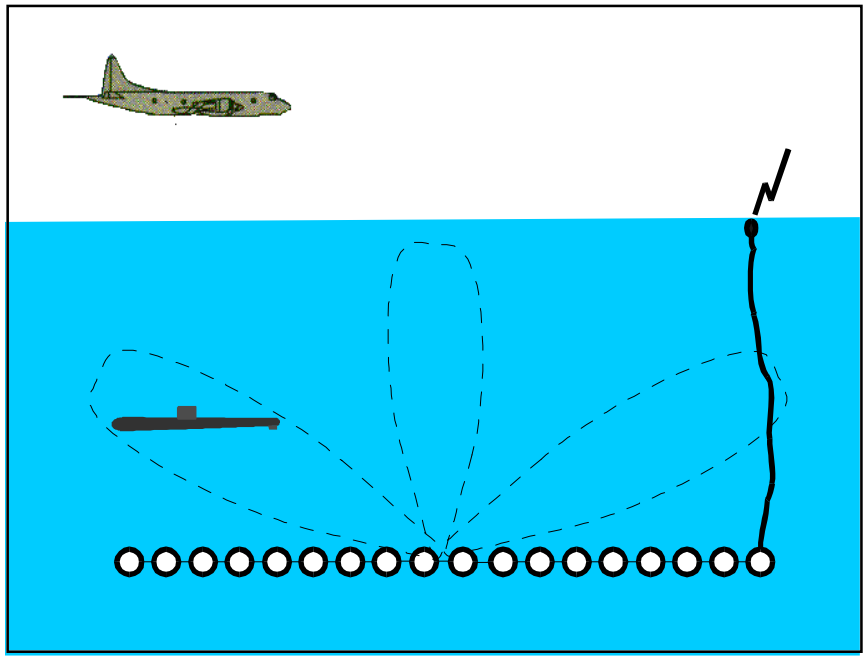
Outline

1. Background
2. Candidate network topologies
3. Node architecture
4. Distributed parallel algorithms and programs
5. Experimental results
6. Integrated simulation environment
7. Conclusions and future research

Background



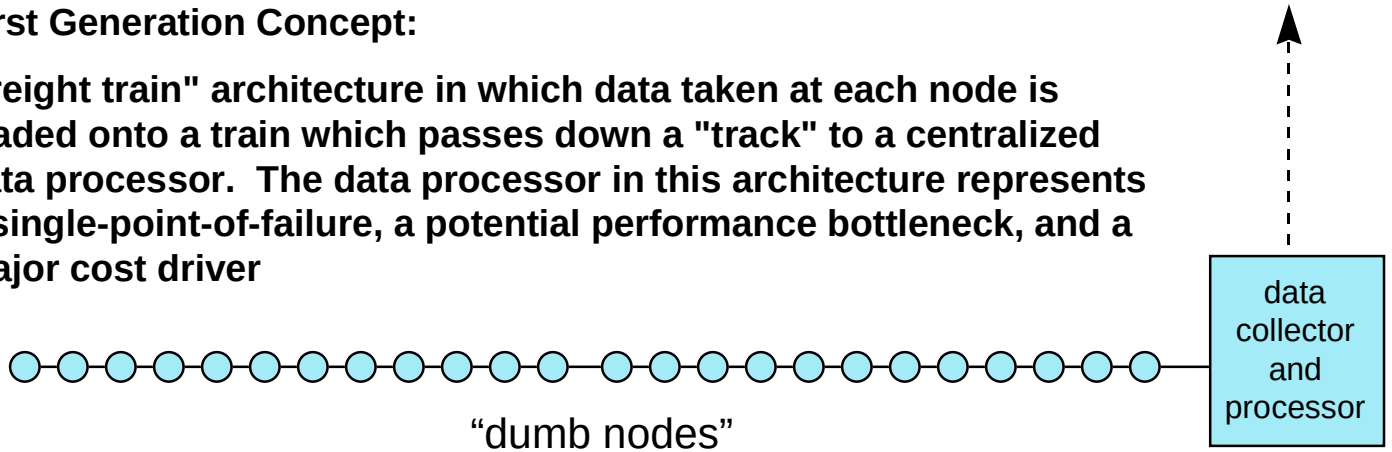
The U.S. Navy is developing a series of disposable air-deployed sonar arrays for undersea surveillance. The arrays must be

- high-gain (high-element-count)
- low-cost
- reliable
- autonomous (in-array processing)
- battery-powered (30-day mission time)

Background (cont.)

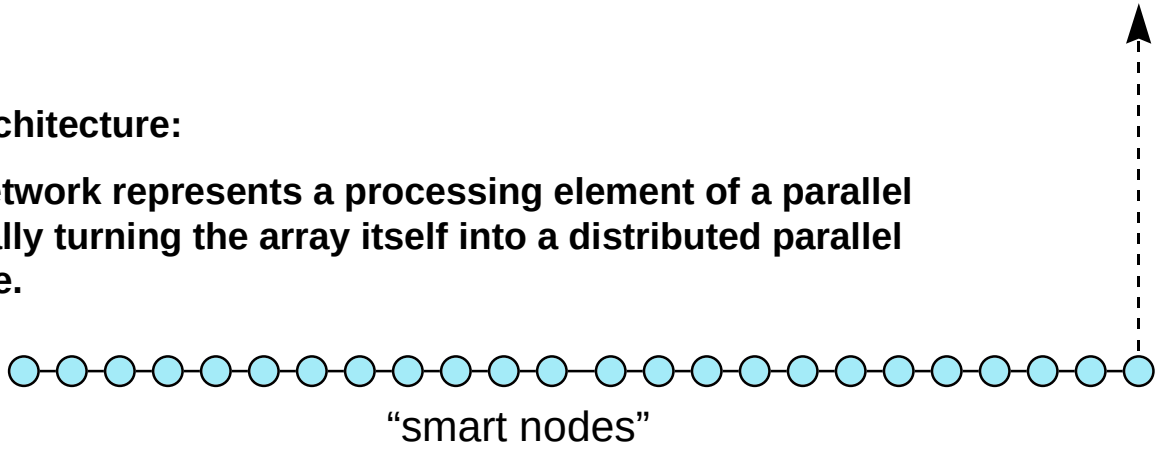
First Generation Concept:

"freight train" architecture in which data taken at each node is loaded onto a train which passes down a "track" to a centralized data processor. The data processor in this architecture represents a single-point-of-failure, a potential performance bottleneck, and a major cost driver



Next Generation Architecture:

each node of the network represents a processing element of a parallel processor, essentially turning the array itself into a distributed parallel processing machine.

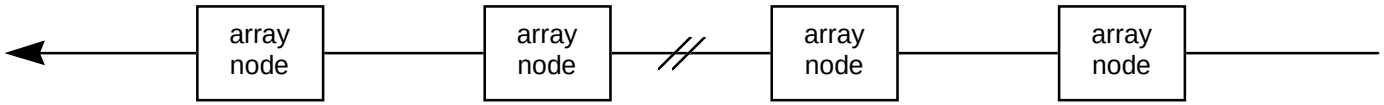


Background (cont.)

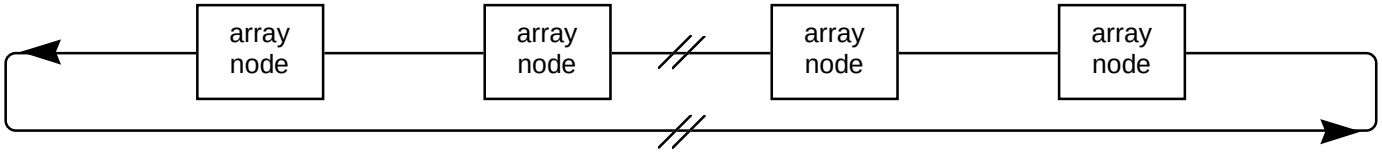
Advantages:

- This approach offers the potential for greatly reduced cost with increased system performance, dependability, and versatility.
- Using the spare processing capacity in the network protocol processors together with the high data rate offered by fiber optics, these improvements can be achieved at essentially no increase to the per-node cost of the array.

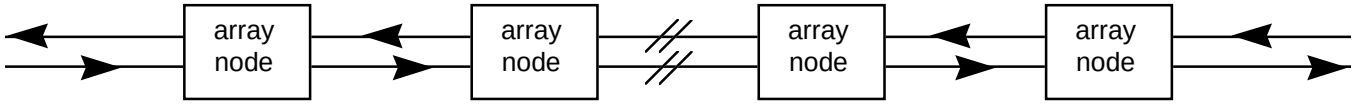
Candidate Network Topologies



(a) uni-directional linear array

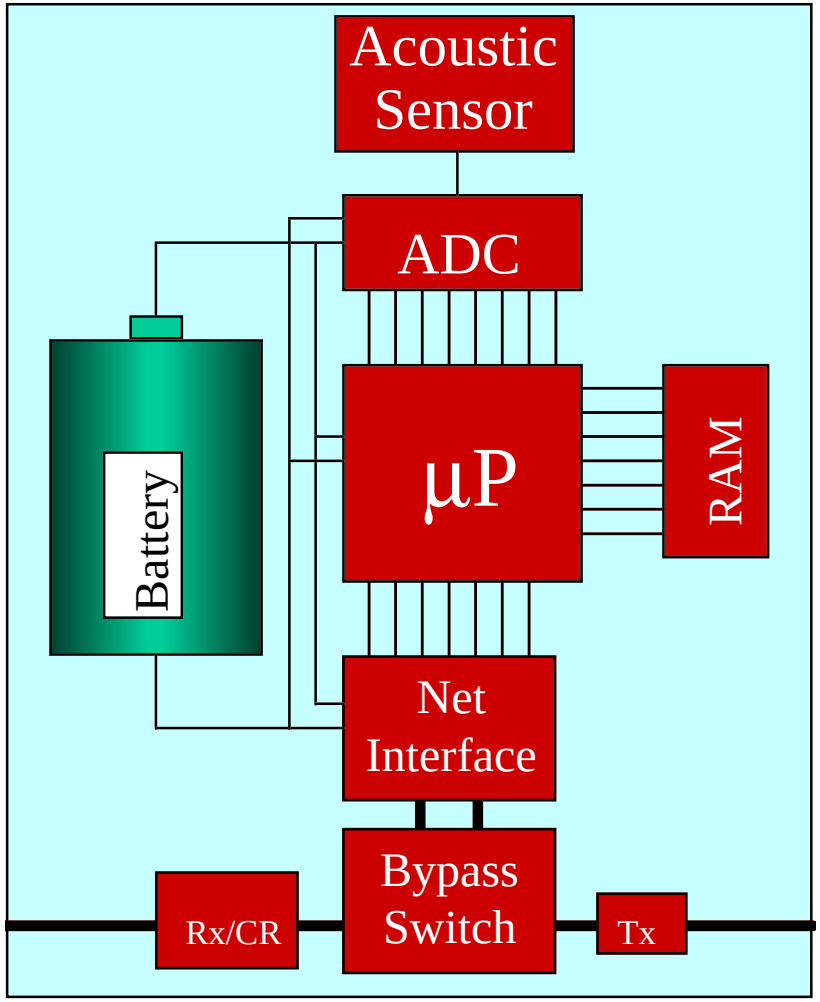


(b) uni-directional ring array



(c) bi-directional linear array

Node Architecture

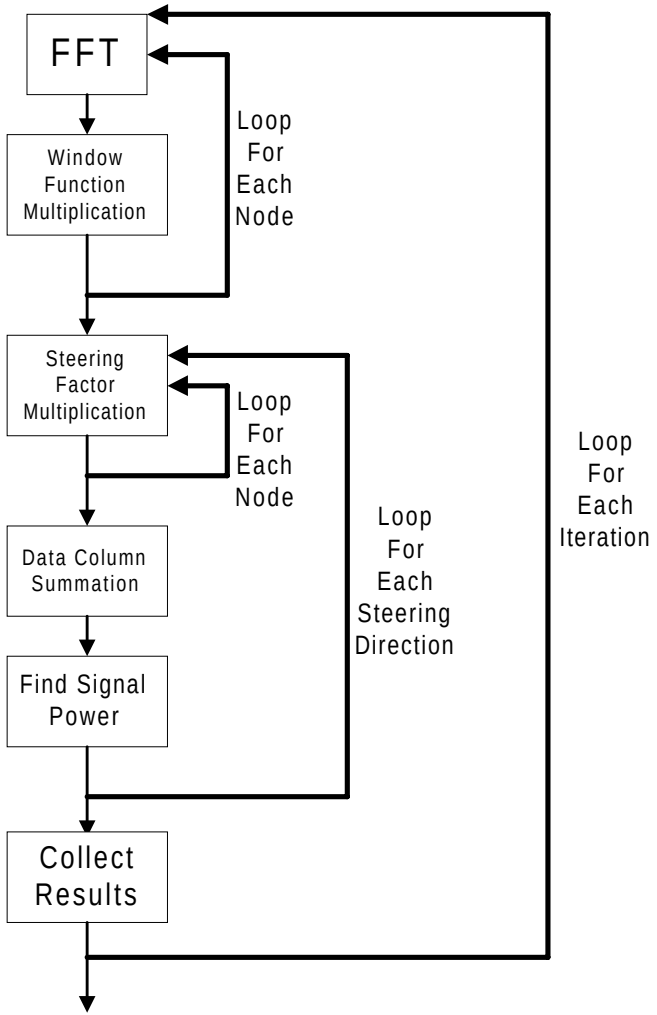


Modeling & Simulation

- **simulates COTS devices (µP, RAM, ADC, etc.) as well as key ASIC characteristics**
- **determines device characteristics for optimal**
  - **performance (MHz, MFLOPS)**
  - **power consumption**
  - **standby-mode usage**
  - **size and weight**
  - **cost**
- **development for hardware prototype**

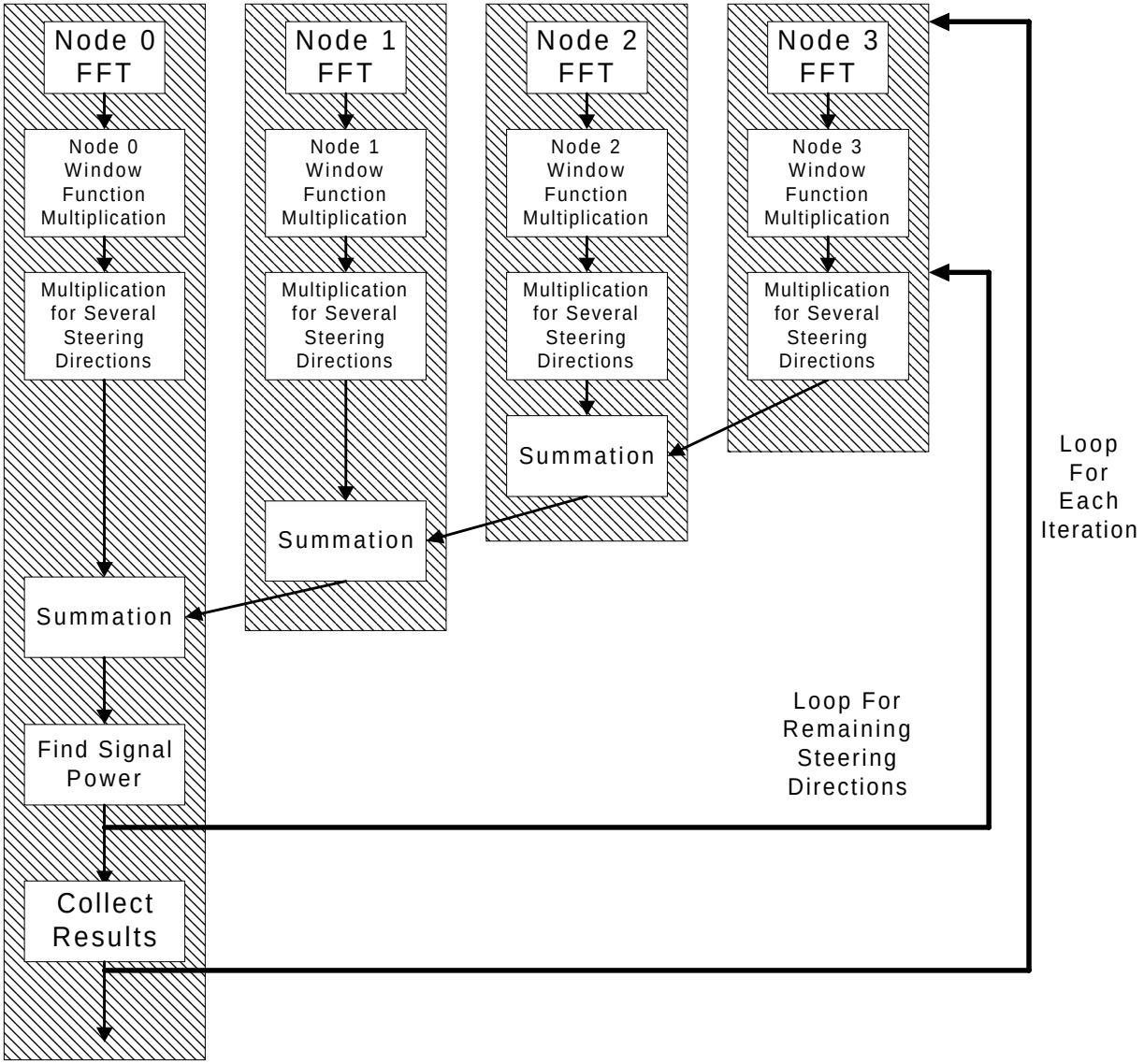
Distributed Parallel Algorithms and Programs

- **decomposition, partitioning, mapping, tuning, and T&E for conventional (both time- and frequency-domain) parallel beamforming algorithms**
- **testbed performance studies provide insight into advantages and disadvantages of each new variant**
- **interrelationships between each promising variant and the candidate node and network architectures are explored**



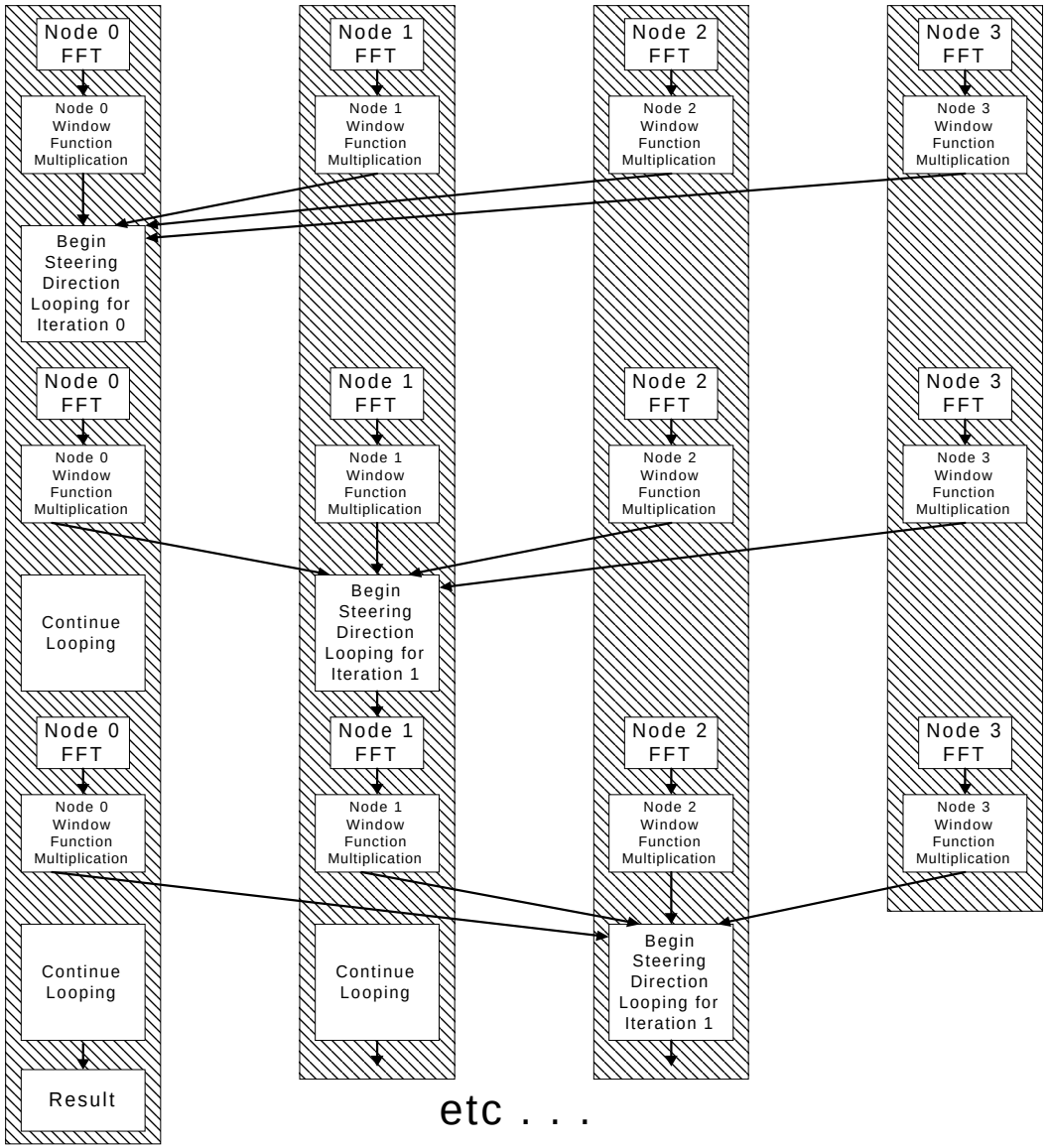
Distributed Parallel Algorithms and Programs (cont.)

Parallel beamformer for uni-directional linear arrays



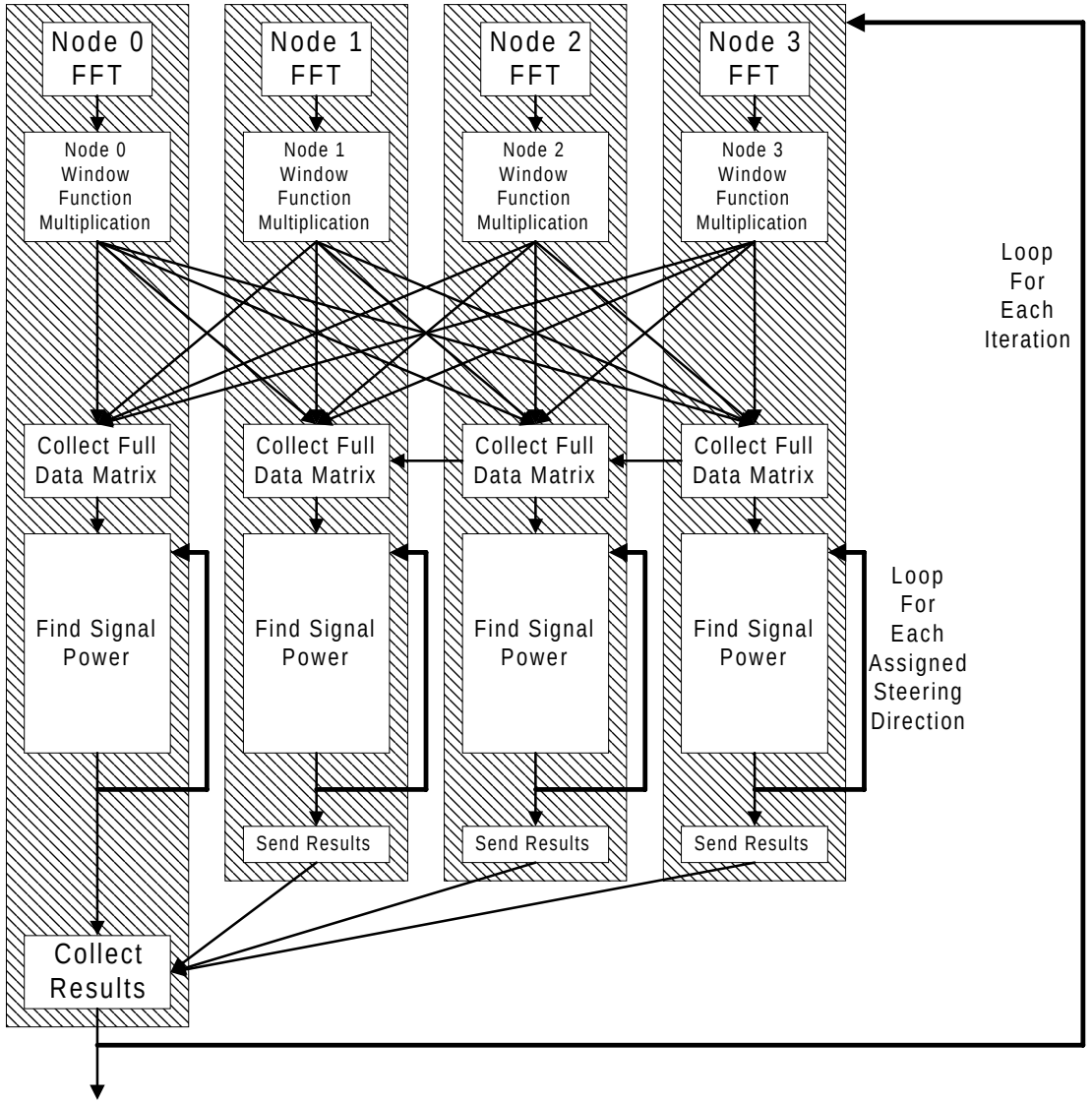
Distributed Parallel Algorithms and Programs (cont.)

Coarse-grain parallel beamformer for bi-directional and ring arrays

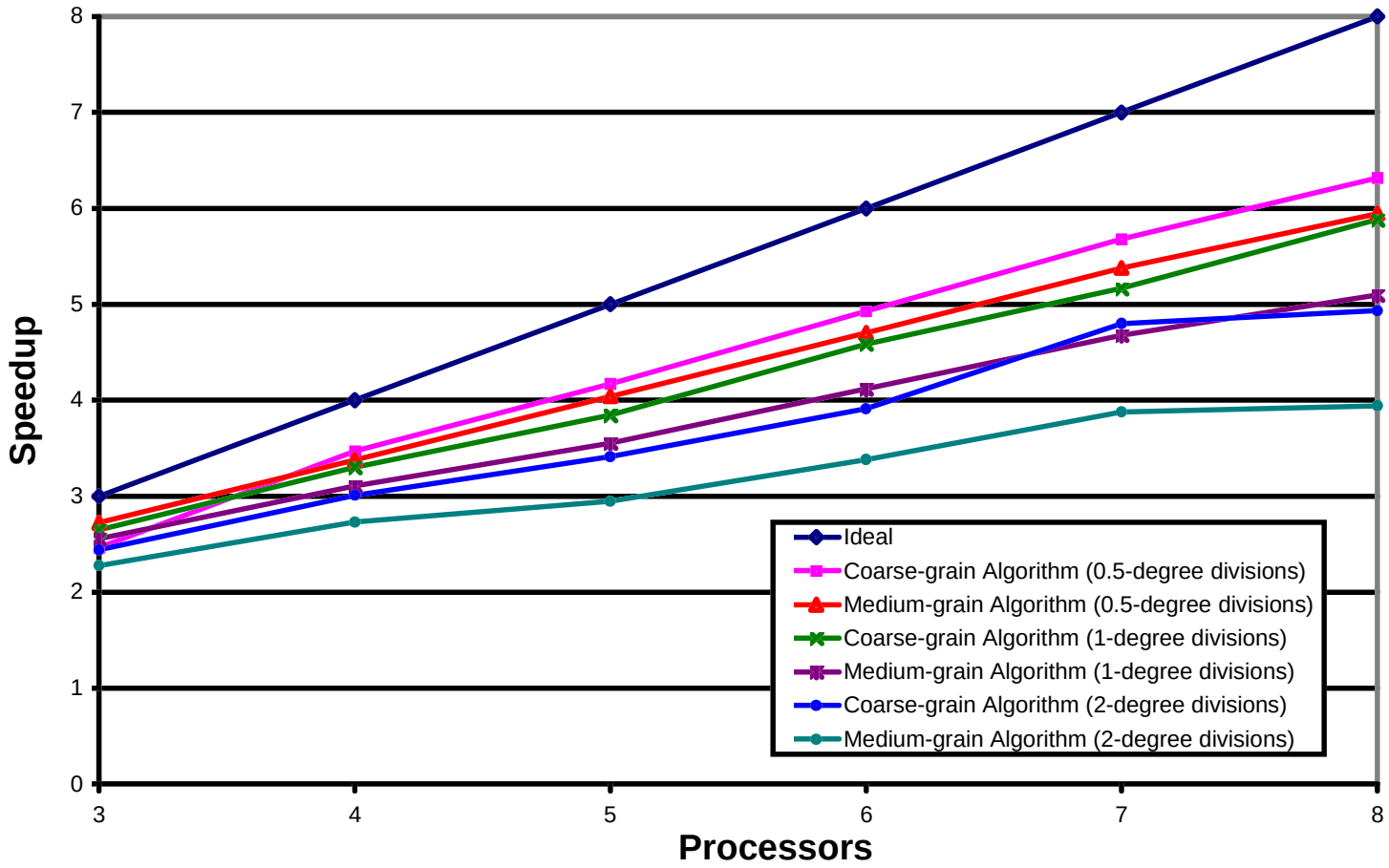


Distributed Parallel Algorithms and Programs (cont.)

Medium-grain parallel beamformer for bi-directional and ring arrays

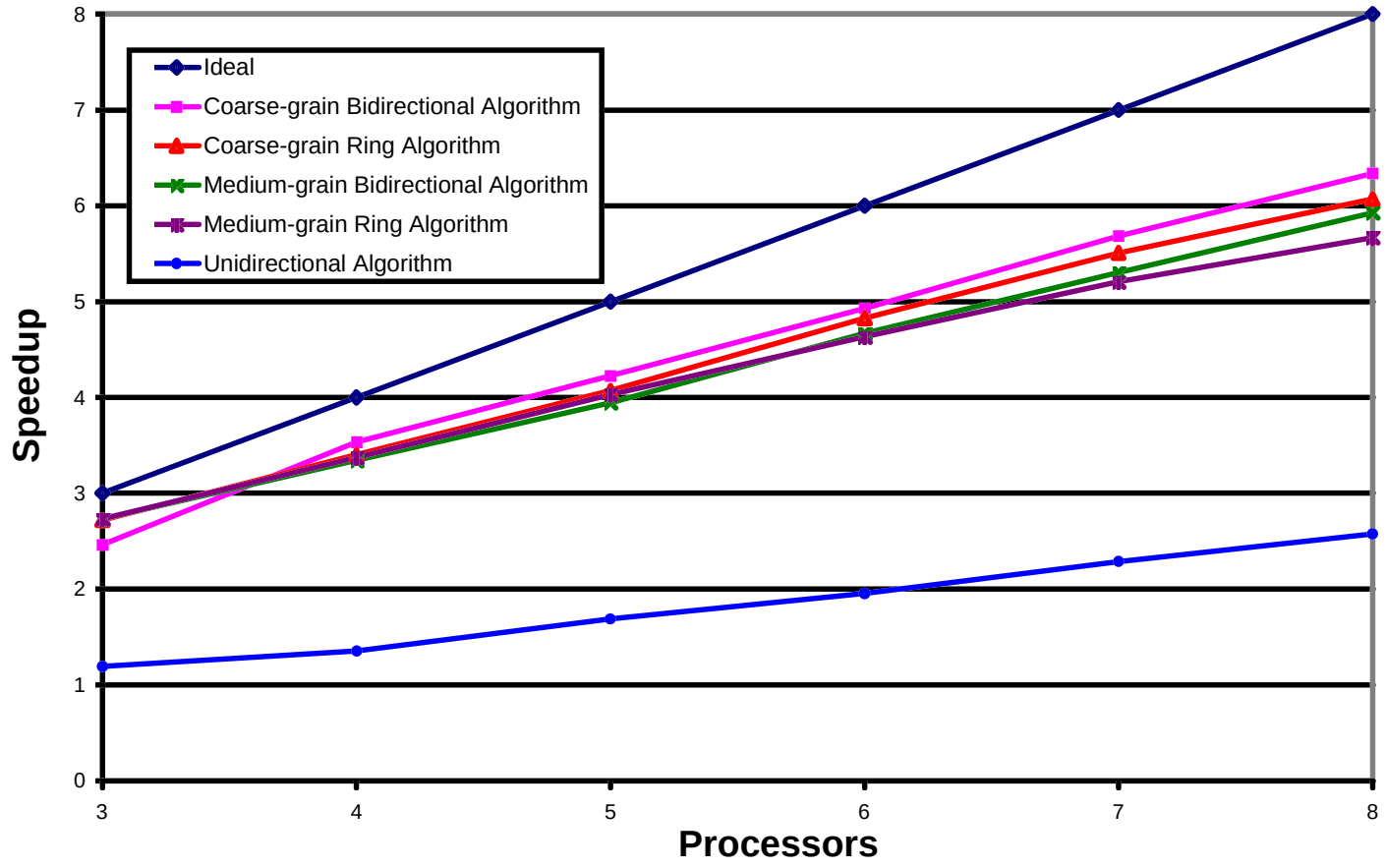


Experimental Results



Performance of coarse- and medium-grain parallel beamformers on a cluster of eight SPARCstation-20/85 workstations connected by OC-3c ATM (155-Mbps), for steering directions from -90 to 90 degrees in increments of 0.5, 1, or 2 degrees

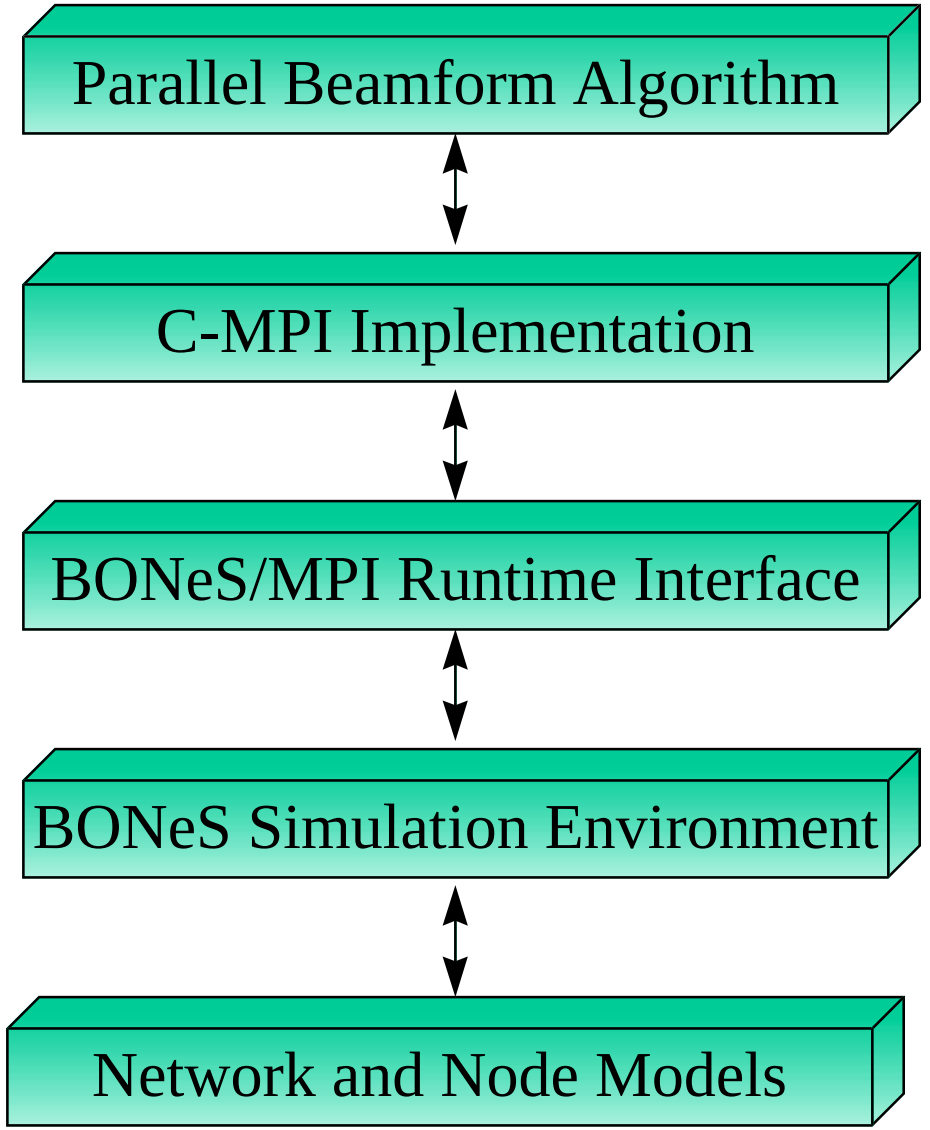
Experimental Results (cont.)



Performance of unidirectional array, ring, and bidirectional array parallel beamformers with network-dependent link-by-link communication on the ATM cluster, for steering directions from -90 to 90 degrees in increments of 0.5 degrees

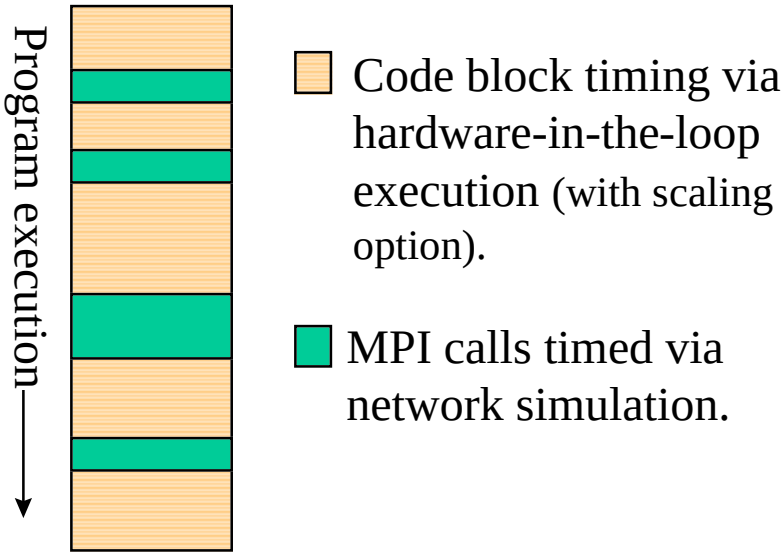
Integrated Simulation Environment (ISE)

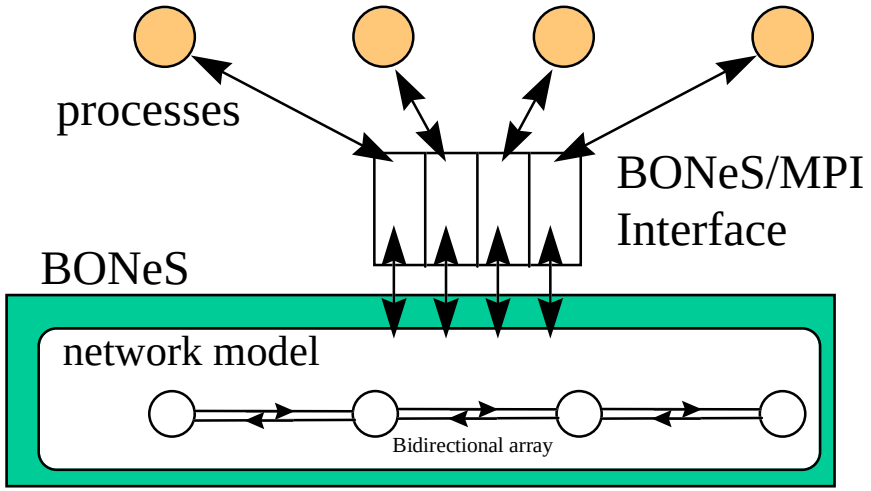
- **Unified design tool for modeling and simulating next-generation sonar arrays and beamforming algorithms**
  - **Rapid virtual prototyping**
  - **Fine-grain system simulation**
  - **Integrates and augments**
    - **Algorithm research**
    - **Network research**
    - **Node architecture research**
  - **Can model current technology and predict performance of future technology**



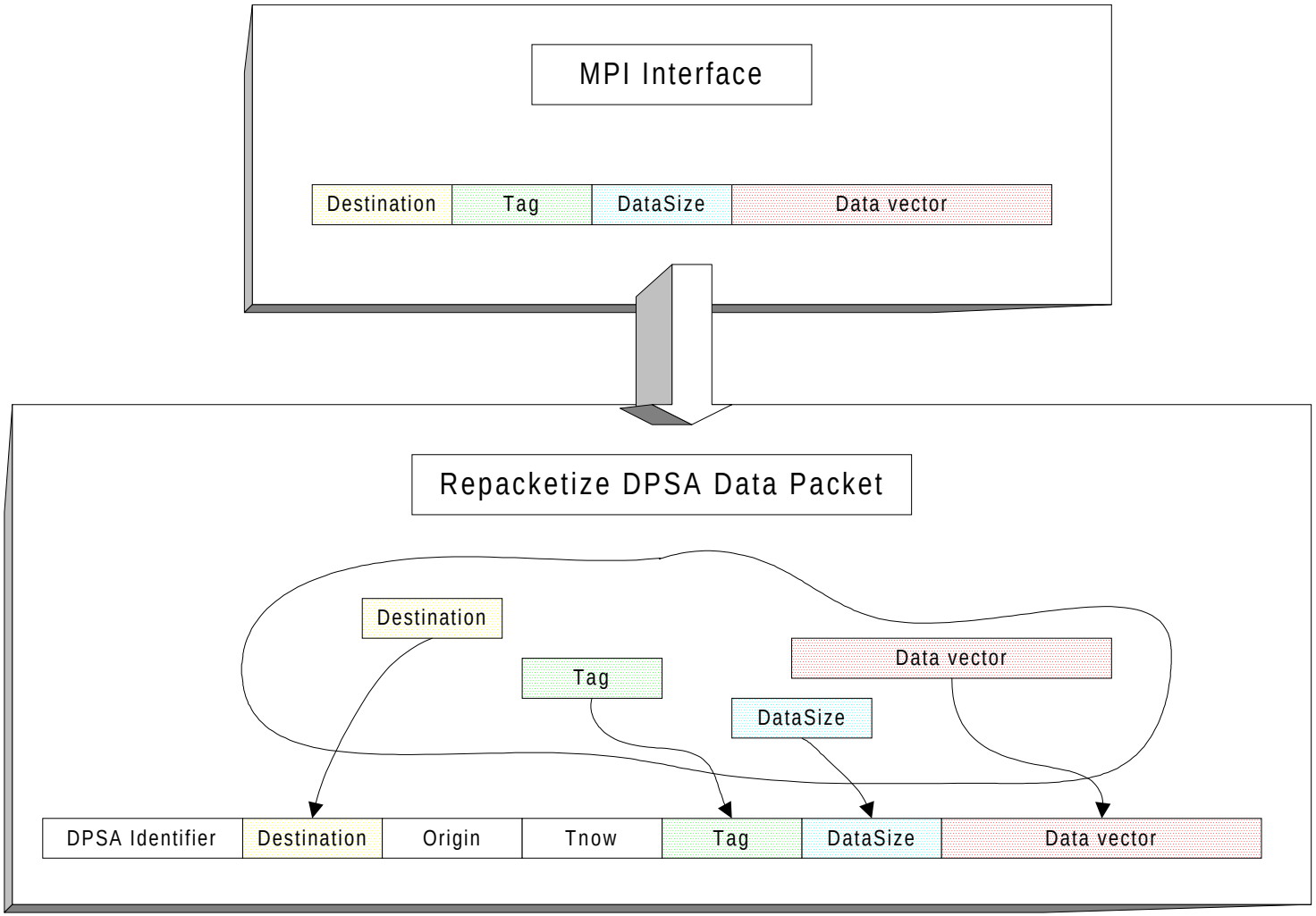
ISE Timing

- **Parallel programs written in unmodified C-MPI code**
- **User process (via BONeS/MPI calls) informs BONeS how long code block computation takes**
- **BONeS will simulate the communication, informing the process when complete**
- **Thus, both HWIL computation and simulated communication are taken into consideration for prototype development**

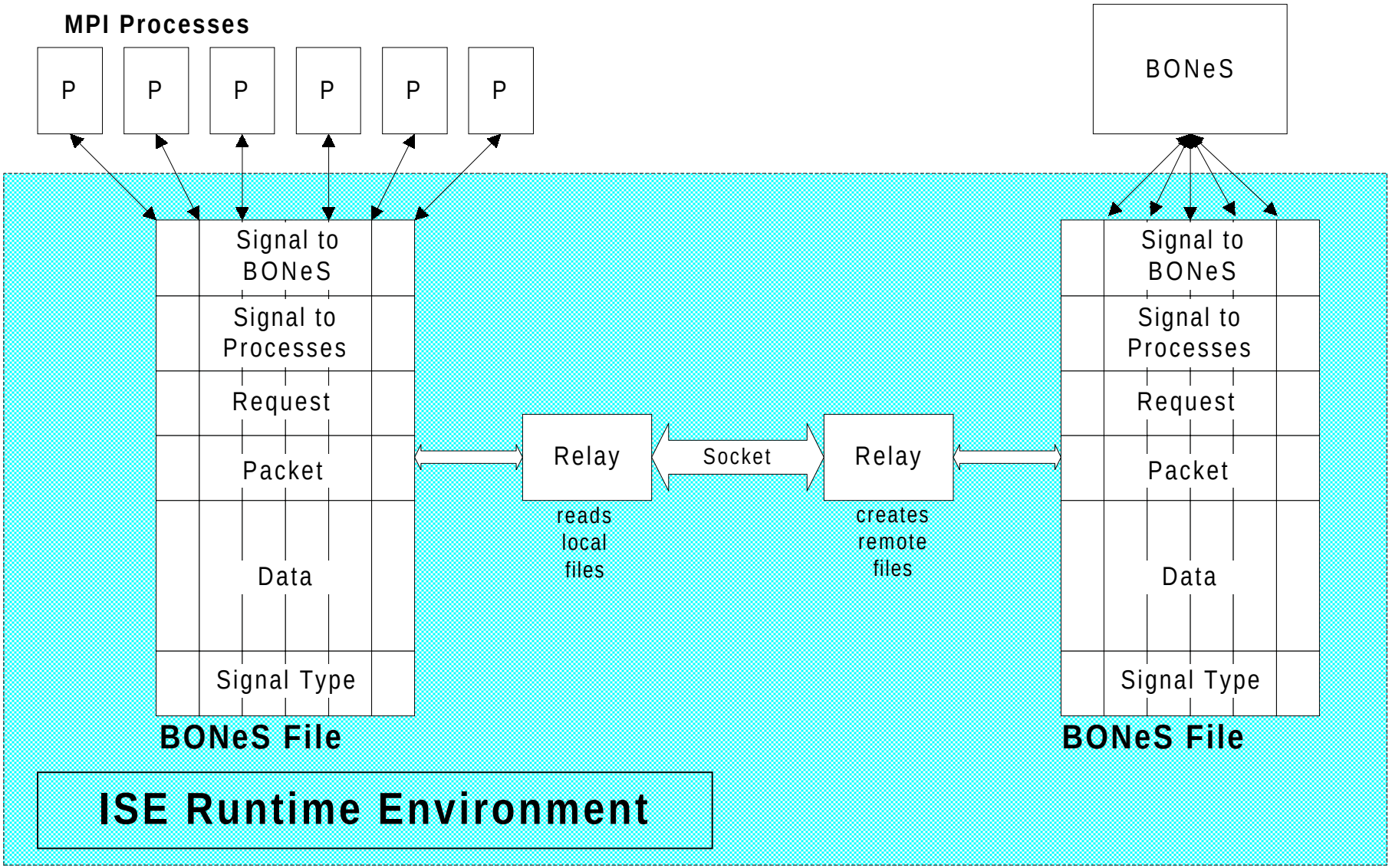




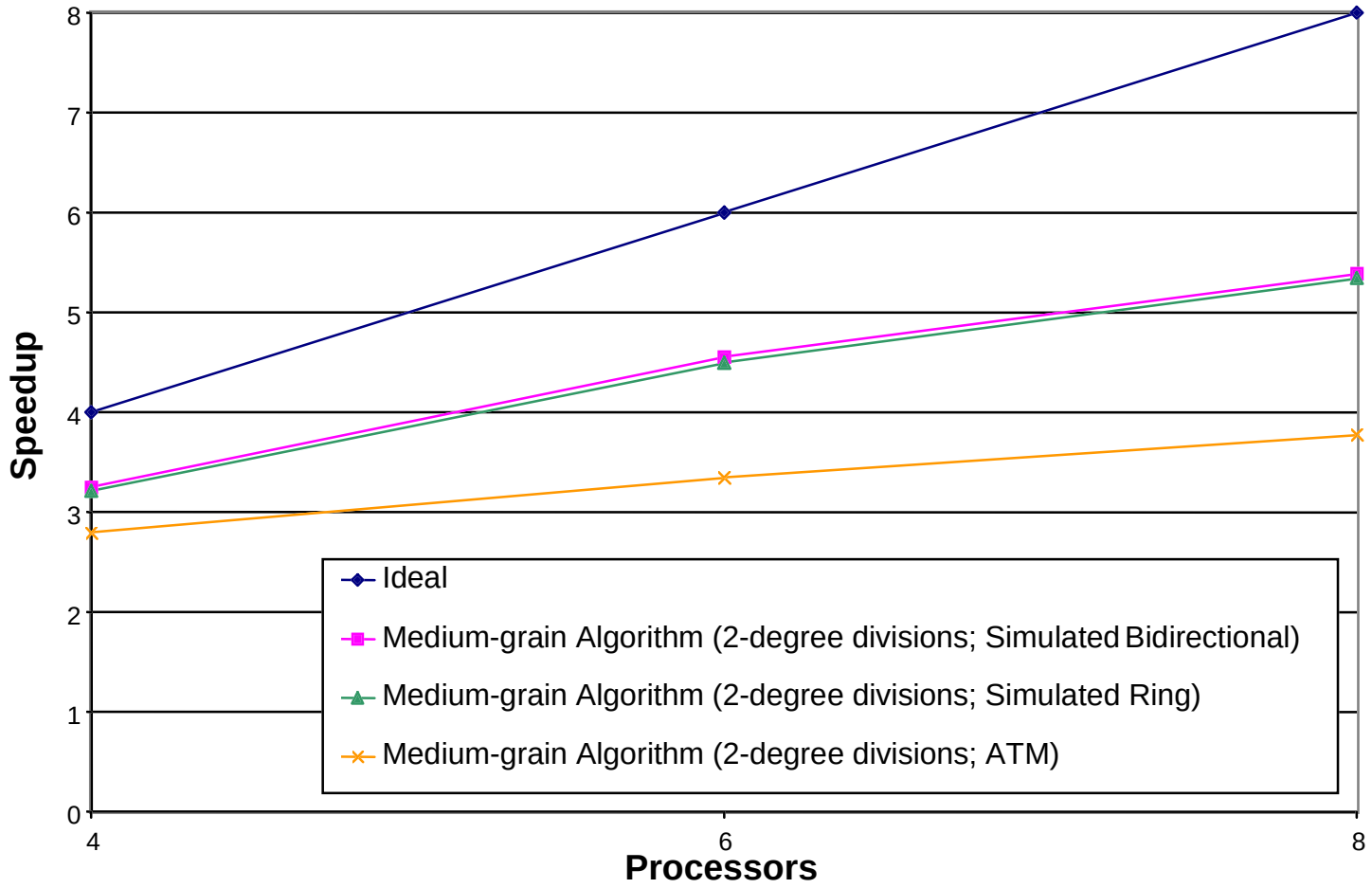
ISE MPI/BONeS Parameter Vectoring



ISE Runtime Environment



Preliminary ISE Results



Performance of medium-grain parallel beamformer both on a cluster of eight UltraSPARC-2/200 workstations connected by OC-3c ATM (155-Mbps) and on UltraSPARC-HWIL ISE, for increments of 2 degrees

ISE Advantages

- **Existing and new beamforming programs can be simulated on nonexistent platforms; thus dozens of systems may be simulated which would be too costly to build**
- **Interface provides a universal glue to which any MPI programs can attach to a simulated network**
- **Real application data flows, so programs are validated as well. Conversely, working applications may effectively be used to debug and improve network protocols**
- **Although BONeS/MPI is run on Sun workstations, the ISE may simulate many architectures and processors by scaling the performance of the SPARC code block measurements**

Conclusions and Future Research

- The use of distributed and parallel processing techniques will reduce the size and cost and improve the performance and reliability of autonomous disposable sonar arrays.
- The performance of architectures based on uni-directional rings and bi-directional linear networks are comparable.
- Both coarse- and medium-grain parallel algorithms provide near-linear speedup for high-spatial-resolution beamforming, with coarse-grain beamformers performing marginally better at all spatial resolutions.
- An integrated simulation approach can provide a rapid virtual prototyping capability that will further reduce system costs.
- Future plans include extending this work to split-array with cross spectral correlation and adaptive beamforming. A laboratory network prototype is also planned.